have since accounted the great majority of digital logic ICs. N-channel FETs are fabricated in an NMOS process, and P-channel FETs are fabricated in a PMOS process. In the 1980s, complementary-MOS, or CMOS, became the dominant process technology and remains so to this day. CMOS ICs incorporate both NMOS and PMOS transistors.

## 2.2 IC PACKAGING

When the wafer has completed its final process step, it is tested and then sliced up to separate the individual dice. Dice that fail the initial testing are quickly discarded. Those that pass inspection are readied for packaging. A package is necessary for several reasons, including protection of the die and the creation of electromechanical connections with other circuitry. ICs are almost always mounted onto a circuit board, and it is usually difficult to mount unpackaged ICs directly to the board. However, there are special situations in which ICs are not packaged and are directly attached to the board. These cases are often at opposite ends of the technological spectrum. At the low end of technology, ICs can be several process generations behind the current state of the art. Therefore, the relative complexity of mounting them to a circuit board may not be as great. The savings of direct mounting are in space and cost. A common quartz wristwatch benefits from direct mounting, because the small confines of a watch match very well with the space savings achieved by not requiring a package for the IC. These watch ICs use mature semiconductor process technologies. At the high end of technology, some favorable electrical and thermal characteristics can be achieved by eliminating as much intermediate bulk as possible between individual ICs and supporting circuitry. However, the technical difficulties of direct-mounting a leading-edge IC can be challenging and greatly increase costs. Therefore, direct-mounting of all but very low-end electronics is relatively rare.

IC packaging technology has evolved dramatically from the early days, yet many mature package types still exist and are in widespread use. Plastic and ceramic are the two most common materials used in an IC package. They surround the die and its lead frame. The lead frame is a structure of metal wires that fan out from the die and extend to the package exterior as pins for connection to a circuit board. Plastic packages are generally lower in cost as compared to ceramics, but they have poorer thermal performance. Thermal characteristics are important for ICs that handle large currents and dissipate large quantities of heat. To prevent the IC from overheating, the heat must be conducted and radiated away as efficiently as possible. Ceramic material conducts heat far better than plastic.

A very common package is the *dual in-line package*, or DIP, shown in Fig. 2.5. A DIP has two parallel rows of pins that are spaced on 0.1-in centers. Each pin extends roughly 0.2 in below the bottom of the plastic or ceramic body. Pins are numbered sequentially from 1 going left to right along one side and resuming on the opposite side from right to left. There is usually at least one pin 1 marker at one end of the package. It is either a dot near pin 1 or a semicircular indentation on one edge of the package.

DIPs are commonly manufactured in standard sizes ranging from 6 to 48 pins, and some manufacturers go beyond 48 pins. Smaller pin-count devices have 0.3-in wide packages, and larger devices are 0.6 in wide. Because of the ubiquity of the DIP, there are many variations of pin counts and package widths. For many years, the DIP accounted for the vast majority of digital logic packages. Common logic ICs were manufactured in 14- and 16-pin DIPs. Memory ICs were manufactured in 16-, 18-, 24-, and 28-pin DIPs. Microprocessors were available in 40-, 44-, and 48-pin DIPs. DIPs are still widely available today, but their use as a percentage of the total IC market has declined markedly. However, the benefits of the DIP remain: they are inexpensive and easy to work with by hand, eliminating the need for costly assembly tools.

If you were to carefully crack open a DIP, you would be able to see the mechanical assembly of the die and lead frame. This is illustrated in Fig. 2.6. The die is cemented in the center of a stamped

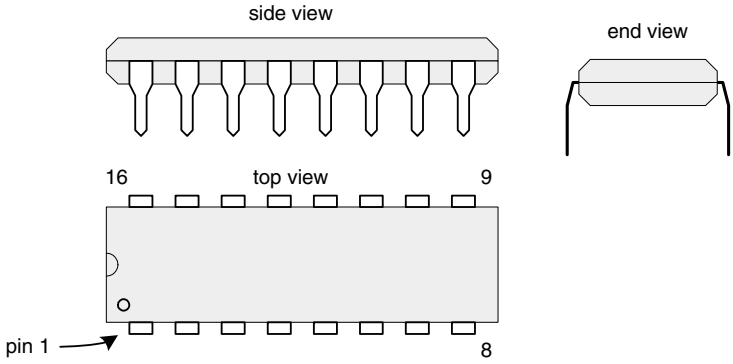


**FIGURE 2.5** A 16-pin dual in-line package.

metal frame and is connected to the individual pins with extremely thin wires. Once the electrical connections are made, the fragile assembly is encased in a plastic or ceramic body for protection and the exterior portions of the pins are folded vertically.

All other IC packages are variations on this theme. Some packages use a similar lead-frame structure, whereas more advanced packages utilize very high-quality miniature circuit boards made from either ceramic or fiberglass.

An oft-quoted attribute of ICs is that their density doubles every 18 months as a result of improvements in process technology. This prediction was made in 1965 by Dr. Gordon Moore, a co-founder of Intel. It has since come to be known as *Moore's law,* because the semiconductor industry has matched this prediction over time. Before to the explosion of IC density, the semiconductor industry classified ICs into several categories depending on the number of logic gates on the device: *small-scale integration* (SSI), *medium-scale integration* (MSI), *large-scale integration* (LSI), and, finally, *very large-scale integration* (VLSI). Figure 2.7 provides a rough definition of these terms. As the density of ICs continued to grow at a rapid pace, it became rather ridiculous to keep adding words like "very" and "extra" to these categories, and the terms' widespread use declined. ICs are now often categorized based on their minimum feature size and metal process. For example, one might refer to an IC as "0.25 μm, three-layer metal (aluminum)" or "0.13 μm, six-layer copper."

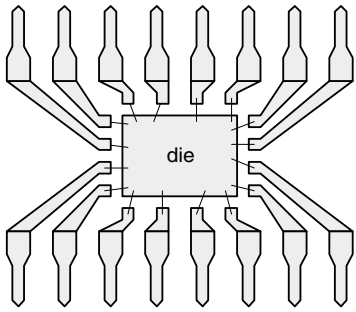


**FIGURE 2.6** DIP lead frame.